Conference Reports

2nd IEEE Latin American Test Workshop

The IEEE Latin American Test Workshop (LATW) was created to address the growing variety of electronic system applications that affect many aspects of modern life. Even as increases in system complexity make it more difficult to protect against manufacturing and field failures, the economic and safety impacts these system have make it all the more critical to do so. In this context, this workshop is a forum for specialists in test technology worldwide, but especially from Latin America, to present and discuss aspects of system, board, and component testing with design, manufacturing, and field considerations in mind. Additionally, this event offers an opportunity for the Latin-American test community to exchange ideas and strengthen relationships.

LATW is sponsored by the Test Technology Technical Council (TTTC) of the IEEE Computer Society and is an important activity of TTTC Latin America. The first workshop was held in 11-14 March 2000 in Rio de Janeiro, Brazil. This year, the second workshop was held in Cancun, Mexico, 11-14 February. The organizers collaborated on the event with the National Institute for Astrophysics, Optics, Electronics-INAOE; and the National Council for Science and Technology-Conacyt. The program committee consisted of members from Latin America, Europe, and North America. Presenters came from Argentina, Belgium, Brazil, the Czech Republic, England, France, Germany, Greece, Italy, Mexico, Portugal, Spain, Taiwan, the Netherlands, and the US.

The technical program included 14 paper sessions covering all aspects of testing technology, two panel sessions, two invited sessions, and two tutorials. The IEEE Computer Society Test Technology Education Program (TTEP) offered two programs: "Design for Testability Techniques: A Comparative Analysis," given by Miron Abramovici, and "Testing Embedded Core-Based Systems Chips," given by Yervant Zorian.

The first panel session covered "Microelectronics Education and Research between Scientific Objectives and Industry Needs," moderated by Magdy Abadir. The second panel was "SOCs Reliability: Oldies or New Stuff?" moderated by Bernard Courtois. Mani Soma gave an invited talk, "Mixed-Signal RF Design-for-Test: Is It R (Real) or F (Fake)?" Joan Figueras gave the second invited talk, "Test Challenges in Nanometrics Technologies."

The Third IEEE Latin American Test Workshop is scheduled for 10-13 February 2002 in Montevideo, Uruguay.

ISQED 2001

The Second IEEE International Symposium on Quality Electronic Design (ISQED 2001) was held on 26-28 March, at the DoubleTree Hotel, San Jose, Calif. Repeating the success of last year's inaugural ISQED, the organizing and technical committees, technical contributors, and speakers made tremendous efforts to make this a premier conference and a valuable event.

ISQED's mission is to promote communication and close cooperation between all the disciplines involved with electronic design. So it was encouraging to see participation not only from the design community but also from other disciplines like electronic design automation, software development, and semiconductor design/manufacture.

In his opening remarks, Ali Iranmanesh, ISQED founder and chair, said that "As ISQED enters its third year, I remain confident that to achieve total design quality, the design process needs to be critically reexamined, and time-proven quality principles and measures should be applied not only to the manufacturing process, but also to design tools and methodologies, design processes, and infrastructures." He stressed that ISQED's vision remains to pro-

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mote and facilitate quality metric development for quantitative quality assessment; develop standards and procedures for quality design; and standards for tools, flows, processes, and infrastructures.

Plenary sessions

Chi-Foon Chan, president and COO of Synopsys, and a member of the ISQED advisory committee, chaired the first plenary session. Hajime Sasaki, chair of NEC, was the first keynote speaker. In his speech, "Future Platform for Mobile Communication," Sasaki described power consumption as a major concern in future adoption of mobile communications platforms. He also stressed that mobile communications devices will soon supplant the PC as the main driver of semiconductor industry growth.

Joe Costello, chair and CEO of think3, gave a speech on "Delivering Quality Delivers Profits." Costello defined system-on-chip quality as "first-silicon success." SOC is the fastest growing design segment because of consumer-driven marketplace demands, Costello said. Raul Camposano, CTO and general manager of Synopsys, outlined the principal types of formal verification techniques in "The Expanding Use of Formal Techniques in Electronic Design."

Edward Ross, president, TSMC USA, spoke of "IC Design Methodology in the Foundry Era: Introducing 'Heads-Up' Design." Ross discussed emerging trends in the EDA, intellectual property, library, and design center communities. In these areas, deep collaboration with foundries is producing a variety of Internet-based solutions that are revolutionizing IC design methodologies.

The second plenary session was chaired by Resve Saleh, technical program chair; and Kris Verma, plenary committee chair. The first speaker was Wojciech P. Maly, professor, Carnegie Mellon University, who talked about "Quality of Design from an IC Manufacturing Perspective." After that, Vinod Agrawal, CEO of Logic Vision, described "Embedded Test Leads to Embedded Quality."

Aki Fujimura, COO and president of Simplex, spoke of "Quality on Time." The final speaker was Philippe Magarshack, vice president, central R&D group, and director, design automation for ST Microelectronics, with his talk, "Quality of SOC Designs Through Quality of the Design Flow: Status and Needs." Videotape and presentation slides of all the plenary speakers will be available through the conference Web site at http://www.isqed.org.

Panels

Three panel discussions with over 20 top specialists covered design topics and issues. The first, "The 50-Million Transistor Chip: The Quality Challenge for 2001," was organized by Rick Merrit and moderated by Richard Goering, both of *EETimes*. Panelists included Thomas Daniel of LSI Logic, Bryan Hoyer of Altera, Chris Malachowsky of Nvidia, Janusz Rajski of Mentor Graphics, Greg Spirakis of Intel, and Tom Williams of Synopsys. The panel explored the growing complexity of verification in electronic design and attempted to answer a provocative question: How much verification is enough?

The second panel discussion was organized by Bill Alexander, and moderated by Jacques Benkowski, both from Monterey Design Systems. This panel discussed "0.13 Micron: Will the Speed Bumps Slow the Race to Market?" Panel participants were Jim Ballingall of UMC USA, Guy Dupenloup of LSI Logic, Dave Hanson of PDF Solutions, Christian Herdt of Compaq Computer, Charlie Huang of CadMos, and Atul Sharan of Numerical Technologies. The panelists shared their experiences, as well as methods and tools that they use to tackle the 0.13-micron challenges and to accelerate design productivity.

Finally, a panel representing scientists, and electronics and design executives shared their visions, experiences, and concerns regarding the impact of electronic design on human life. This panel was entitled "Consequences of Technology—What is the Impact of Electronic Design on the Quality of Life?" The panel was organized by Nader Vasseghi of AuroraNetics and Gabriele Eckert of RubiCad, and was moderated by Steve Ohr of EDTN Networks. Panel participants included Sabrina Kemeny of Photobit, Tom Mahon of Thomas Mahon & Associates, Peter G. Neumann of SRI, Peggy Aycinena of *Integrated Systems Design*, Joe Hall of Clarus, and Bryan Hoyer of Altera.

10th North Atlantic Test Workshop Managing Massive Design and Test Complexities

24-25 May 2001
Ocean View Inn and Resort
Gloucester, Mass.

Sponsored by
the IEEE Computer Society,
the Test Technology Technical Council,
and the University of Mass.

In the past nine years, engineers, researchers, educators, and students representing major technology companies and institutions have attended NATW. The organizing and program committees of this year's workshop invite everyone interested in design and test to share expertise and to experience the NATW spirit of open and unlimited discussions.

Keynote address:
Yervant Zorian of Logic Vision.

Invited Addresses:
Song Lee of Teradyne and Shawn Blanton of Carnegie Mellon University

Introduction on Design Validation:
Dhiraj Pradhan of Oregon State University

Technical presentation sessions:
DFT and BIST
High-level fault modeling
HDL test
Defect analysis and parametric test
System test issues

For information see
http://www.ecs.umass.edu/natw
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Technical papers and awards

Eleven sessions presented a collection of papers about IC design, electronic design automation, test, and equipment from both universities and the semiconductor industry. The program committee accepted 36 papers for oral presentation of the 93 submitted. It accepted an additional 18 papers for poster presentation. The technical program also includes 13 invited papers from leading experts.

ISQED awarded two best papers. Jayant Deodhar of Intel and Spyros Zafkos of Southern Illinois University received an award for their paper, "Color Counting and its Application to Path Delay Fault Coverage." The second award went to Andrew B. Khang and Stefanus Mantik of the University of California at Los Angeles for their paper, "A System for Automatic Recording and Prediction of Design Quality Metrics."

This year ISQED also featured a PhD student forum. The award for best PhD student forum paper went to Tung-Yang Chen and Ming-Dou Ker for their poster paper, "Design on ESD Protection Circuit with Very Low and Constant Input Capacitance."

Tutorials

Due to popular demand, the tutorial sessions expanded to 12 sessions. These sessions covered a variety of critical and timely topics such as embedded test strategies for SOCs design and test of low-voltage CMOS circuits; redundancy requirements for embedded memories; design metrics for achieving design quality; fundamental methods to enable SOC design and reuse; deep-submicron state-of-the-art; and electronic system design, application of formal verification to design creation and implementation, verification and validation of complex digital systems, physical verification of deep-submicron designs, reconnecting MOS modeling and circuit design, interconnect modeling for timing, signal integrity and reliability, and on-chip inductance extraction and modeling.

Future ISQED events

ISQED 2002 will be 18-20 March 2002 in San Jose, Calif. Address inquiries about the conference to isqed@isqed.org. The conference Web site is http://www.isqed.org.